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(54) PATTERNING METHOD FOR SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To enable easy patterning by a process using a photolithographic method.
CONSTITUTION: A layer 5 comprising of SiNx among layers laminated on a substrate 1 is patterned. A patterning substrate 21 is prepared wherein a Cr- based silicide formation material layer 31 is formed by a specified pattern and is thermally compressed to the layer 5. When the patterning substrate 21 is removed, silicide which is a compound of Cr and SiNx is produced on the layer 5 and a silicide part 5a is formed. Patterning wherein the silicide part 5a is used as a mask is enabled by dry-etching whose etching rate is different between silicide and SiNx.

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CLAIMS

[Claim(s)]

[Claim 1] About the 1st layer which consists of the 1st ingredient which constitutes the semiconductor device in the middle of a production process It is the patterning approach of the semiconductor device which forms a predetermined pattern by removing the part. So that the substrate for patterning in which the 2nd layer which consists of the 2nd ingredient is formed by said predetermined pattern may be prepared and said the 1st layer and said 2nd layer may come into contact with mutually Contact said substrate for patterning to said semiconductor device, and the predetermined conditions that a chemical reaction occurs by contact into said 1st ingredient and said 2nd ingredient are maintained. After generating both compound in the contact section of said 1st ingredient and said 2nd ingredient and removing said substrate for patterning, by the etching approach that the etching rates between said 1st ingredient and said compounds differ The patterning approach of the semiconductor device characterized by carrying out etching removal of said a part of 1st layer.

[Claim 2] The patterning approach of the semiconductor device characterized by making it make silicide generate as a compound in the patterning approach according to claim 1, using silicon as the 1st ingredient or 2nd ingredient.

[Claim 3] The patterning approach of the semiconductor device characterized by using the layer which constitutes a part of thin film transistor as the 1st layer in the patterning approach according to claim 1.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the patterning approach of a semiconductor device, and the patterning approach which was suitable for manufacture of a thin film transistor, a solar battery, various sensors, etc. especially.
[0002]
[Description of the Prior Art] A common semiconductor device has the structure to which the laminating of two or more layers was carried out by respectively various patterns on a semi-conductor substrate. For this reason, in the production process of a semiconductor device, formation of the layer to a semi-conductor substrate top and patterning to the formed layer are performed repeatedly. The most general patterning approach used conventionally is the photolithography method. By this approach, a resist layer is formed on the layer used as a patterning object, where the mask with which the predetermined pattern was drawn on this resist layer is carried, it exposes, and a resist layer is developed, a part for an exposure part or a non-exposed area is removed, and etching of the layer for patterning is performed, using the resist layer which remained as a protective coat.
[0003]
[Problem(s) to be Solved by the Invention] By the photolithography method mentioned above, in order to carry out patterning of the one layer which is applicable, four phases of formation of ** resist layer, the exposure which used ** mask, the development of ** resist layer, and ** etching are needed. By the time it generally completes all manufacture processes since patterning to many layers is needed in order to manufacture one semiconductor device, complicated processing which consists of many phases very much must be performed. For this reason, manufacture took time amount and there was a problem that cost also became high.

[0004] Then, this invention aims at offering the patterning approach of a semiconductor device that a simpler process can perform patterning.
[0005]
[Means for Solving the Problem] In the patterning approach of the semiconductor device which forms a predetermined pattern by removing the part about the 1st layer which this invention becomes from the 1st ingredient which constitutes the semiconductor device in the middle of a production process So that the substrate for patterning in which the 2nd layer which consists of the 2nd ingredient is formed by the predetermined pattern may be prepared and the 1st layer and 2nd layer may come into contact with mutually Contact the substrate for patterning to a semiconductor device, and the predetermined conditions that a chemical reaction occurs by contact into the 1st ingredient and the 2nd ingredient are maintained. After generating both compound in the contact section of the 1st ingredient and the 2nd ingredient and removing the substrate for patterning, it is made to carry out etching removal of a part of 1st layer by the etching approach that the etching rates between the 1st ingredient and a compound differ.
[0006]
[work --] for The patterning approach concerning this invention imprints a pattern in the way which pushes a stamp so to speak. That is, the 2nd layer is beforehand formed in the substrate for patterning which plays the role of the stamp version by the predetermined pattern. The pattern formed in this 2nd layer is imprinted in the 1st layer used as a patterning object. The 2nd layer and 1st layer are contacted and a compound is made to specifically generate among both ingredients by maintaining at predetermined temperature etc. On the 1st layer, in order for a compound to be generated by only the part in contact with the 2nd layer, the pattern image of the stamp version will be imprinted. If etching from which it is after this with the part by which the compound was generated, and the other part, and an etching rate differs is performed, etching as the pattern image of the stamp version will be performed. According to this approach, patterning to one layer is completed by two steps of processings of the imprint of ** pattern, and ** etching.
[0007]
[Example] Hereafter, it explains based on the example illustrating this invention. Here, the example which applied this invention to the manufacture process of a thin film transistor will be explained. Drawing 1 - drawing 13 are the sectional views showing the manufacture process of this thin film transistor in order. First, as shown in drawing 1 ,

the gate electrode 2 which consists of conductive ingredients, such as aluminum and chromium, is formed on a glass substrate 1. Then, as shown in drawing 2 , the insulating layer 3 which consists of SiNx etc. is formed on this, the intrinsic-semiconductor layer 4 which consists of a-Si:H (amorphous silicon which added hydrogen) etc. is formed on it, and the etching stopper layer 5 which consists of SiNx etc. is further formed on it. So far, it is completely the same as the production process of the conventional general thin film transistor.

[0008] Then, patterning of the etching stopper layer 5 is performed. Although patterning which used the photolithography method was performed conventionally, the following processings are performed by the patterning method by this invention. First, the substrate [as] 21 (low thermal expansion glass is used in this example) for patterning shown in drawing 3 is prepared. The silicide formation ingredient layer 31 is formed in the front face of this substrate 21 for patterning by the predetermined pattern. So to speak, this substrate 21 for patterning plays a role of a stamp version, and the pattern which should be imprinted in the etching stopper layer 5 is beforehand formed of the silicide formation ingredient layer 31. The silicide formation ingredient layer 31 reacts on condition that the ingredient of the etching stopper layer 5, and predetermined, and consists of ingredients which generate silicide. In this example, the etching stopper layer 5 is SiNx and the silicide formation ingredient layer 31 consists of Cr. In this way, the prepared substrate 21 for patterning is pushed against the top face of the etching stopper layer 5 as shown in the arrow head of drawing 3 , and it is made for the silicide formation ingredient layer 31 to contact the etching stopper layer 5. Here, temperature is kept at 150-400 degrees C, pushing the substrate 21 for patterning by a certain amount of pressure. If the substrate 21 for patterning is removed as shown in drawing 4 after performing such thermocompression bonding, silicide section 5a will be generated by the contact section of the etching stopper layer 5 and the silicide formation ingredient layer 31. That is, as a result of performing thermocompression bonding, silicide (Cr3Si, Cr2Si3, etc.) is generated by the chemical reaction of SiNx and Cr as both compound. It means that the stamp mark (silicide section 5a) was formed in the front face of the etching stopper layer 5 by pushing a stamp by the substrate 21 for patterning as a stamp version so to speak.

[0009] In addition, although this application drawing does not show the thickness of the expedient top of explanation, and each class by the ratio of an absolute size, in fact, the thickness (for example, about 1 micrometer) of the silicide formation ingredient layer 31 is fully thick

compared with the thickness (for example, about 0.05 micrometers) of the etching stopper layer 5, and the thickness of the substrate 21 for patterning is still thicker (for example, about 1mm). Therefore, it is possible for it to be almost changeless to the silicide formation ingredient layer 31 side, and to perform thermocompression bonding processing by them repeatedly to many etching stopper layers 5 using the same substrate 21 for patterning, even if silicide section 5a is generated by the above thermocompression bonding processings at the etching stopper layer 5 side. Therefore, once it creates the substrate 21 for patterning as a stamp version (what is necessary is just to create this by the conventional photolithography method etc.), imprint processing of a pattern can be performed to many semiconductor devices.

[0010] Now, if the imprint of a pattern is completed as silicide section 5a as shown in drawing 4 , etching processing to the etching stopper layer 5 can be performed by using this silicide section 5a as a mask. That is, if processing which carries out etching removal of a part of etching stopper layer 5 is performed using the etching approach that the etching rates between the etching stopper layer 5 and silicide section 5a differ, as shown in drawing 5 , it can leave a part of etching stopper layer 5 as etching stopper section 5b. What is necessary is just to perform dry etching which exposes the etching stopper layer 5 to the ambient atmosphere which plasma-ized etching gas, such as SF6 and CF4, as such an alternative etching approach. In such dry etching, since the etch rate of SiNx becomes large 10 or more times compared with silicide, silicide section 5a can be used as substitution of a mask.

[0011] The description of the patterning approach by this invention is in the point of performing patterning to the etching stopper layer 5, by two steps of processings of the imprint (thermocompression bonding by the substrate 21 for patterning) of ** pattern, and ** etching (alternative etching using silicide section 5a generated by ** as a mask), as mentioned above. Compared with patterning by the conventional photolithography method, a routing counter can decrease and can shorten the processing time.

[0012] Then, explanation of the production process of a thin film transistor can be progressed further. The next processing is processing which performs patterning to the intrinsic-semiconductor layer 4 in the condition which shows in drawing 5 . Too, although patterning which used the photolithography method was performed conventionally, the following processings are performed by the patterning method by this invention. First, the substrate 22 for patterning as shown in drawing 6 is prepared. The silicide formation ingredient layer 32 is formed in the front face

of this substrate 22 for patterning by the predetermined pattern, and a pattern imprint is performed in the intrinsic-semiconductor layer 4, using this substrate 22 for patterning as a stamp version. Too, the silicide formation ingredient layer 32 reacts on condition that the ingredient of the intrinsic-semiconductor layer 4, and predetermined, and consists of ingredients (this example Cr) which generate silicide. In this way, the prepared substrate 22 for patterning is pushed against the top face of the intrinsic-semiconductor layer 4 as shown in the arrow head of drawing 6 , and it is made for the silicide formation ingredient layer 32 to contact the top face of etching stopper section 5b and the intrinsic-semiconductor layer 4. As mentioned above, it compares with the level difference (about 0.05 micrometers) which the actual thickness of the silicide formation ingredient layer 32 is about 1 micrometer, and was formed in the thickness and the intrinsic-semiconductor layer 4 of etching stopper section 5b. In addition, since it is very thick, According to the level difference formed in the semiconductor device top face, mechanical bending arises in the silicide formation ingredient layer 32, and the silicide formation ingredient layer 32 can contact homogeneity mostly on the top face of etching stopper section 5b and the intrinsic-semiconductor layer 4. Thermocompression bonding is performed again here, keeping temperature at 150-400 degrees C. Then, as shown in the contact section of the intrinsic-semiconductor layer 4 and the silicide formation ingredient layer 32 at drawing 7 , silicide section 4a is generated. Then, if processing which carries out etching removal of a part of intrinsic-semiconductor layer 4 is performed using the etching approach that the etching rates between an amorphous silicon and silicide differ, as shown in drawing 8 , a part of intrinsic-semiconductor layer 4 will remain, and channel layer 4b will be formed. Thus, also in patterning for forming channel layer 4b, if this invention is applied, it will end by processing of only 2 processes.

[0013] Explanation of the production process of a thin film transistor can be progressed further. As shown in drawing 9 , the impurity dope layer 6 (for example, n+ amorphous silicon layer) is made to deposit, and patterning is performed to this impurity dope layer 6. Although patterning which used the photolithography method too was performed conventionally, the following processings are performed by the patterning method by this invention. First, the substrate 23 for patterning as shown in drawing 10 is prepared. The silicide formation ingredient layer 33 is formed in the front face of this substrate 23 for patterning by the predetermined pattern, and a pattern imprint is

performed on the impurity dope layer 6, using this substrate 23 for patterning as a stamp version. Here, the silicide formation ingredient layer 33 reacts on condition that the ingredient of the impurity dope layer 6, and predetermined, and consists of ingredients (this example Cr) which generate silicide. In this way, the prepared substrate 23 for patterning is pushed against the top face of the impurity dope layer 6 as shown in the arrow head of drawing 10 , and it is made for the silicide formation ingredient layer 33 to contact the top face of the impurity dope layer 6. Too, the actual thickness of the silicide formation ingredient layer 33 is about 1 micrometer, and since it is very thick compared with the level difference formed in the impurity dope layer 6, the silicide formation ingredient layer 33 can contact homogeneity mostly to the impurity dope layer 6. In this way, thermocompression bonding is performed, keeping temperature at 150-400 degrees C. Then, as shown in the contact section of the impurity dope layer 6 and the silicide formation ingredient layer 33 at drawing 11 , silicide section 6a is generated. Then, if processing which carries out etching removal of a part of impurity dope layer 6 is performed using the etching approach that the etching rates between an amorphous silicon and silicide differ, as shown in drawing 12 , a part of impurity dope layer 6 will remain, and drain side dope layer 6b and source side dope layer 6c will be formed.

[0014] Now, if drain electrode layer 7a and source electrode layer 7b are formed, then the display electrode layer 8 is finally formed as shown in drawing 13 , generation processing of the basic component of a thin film transistor will be completed. It means carrying out patterning of the etching stopper layer 5, patterning of the intrinsic-semiconductor layer 4, and patterning of 3 passage called patterning of the impurity dope layer 6 by the patterning method by this invention in the above process after all. For this reason, compared with the conventional approach, it is simplified considerably, and time amount and cost can reduce all processes.

[0015] As mentioned above, although explained based on the example illustrating this invention, this invention is not limited only to this example and can be carried out in various modes. Especially as a silicide formation ingredient, although Cr was used in the above-mentioned example, other ingredients may be used. general -- as silicide -- Cu3Si, Cr3Si, nickel3Si, calcium3Si2, Fe3Si2, Co3Si2, nickel3Si2, Cr2Si3, Mo2Si3, and W2 -- Si3 and nickel2 -- Si3, CoSi3, etc. are known and, in short, a binary compound with a positivity element (especially metallic element) serves as silicide from silicon and it electrically.

Therefore, as a silicide formation ingredient, metals other than Cr, such as calcium, Fe, Co, nickel, Cu, Mo, and W, can be used. Moreover, in order to carry out patterning of the metal layers, such as Cr, you may make it use the stamp version with which the silicide formation ingredient layer which consists of silicon was formed completely contrary to this, although the stamp version with which the silicide formation ingredient layer which consists of Cr was formed is used in the above-mentioned example in order to carry out patterning of the silicon layer. Moreover, a silicon layer is not a required reason and does not necessarily need to generate silicide as a compound. In short, when performing patterning about the 1st layer which consists of the 1st ingredient, this invention The stamp version is created by the 2nd layer which consists of the 2nd ingredient with a property which generates a compound by making it contact on these the 1st ingredient and predetermined conditions. Unless it deviates from this technical thought based on the technical thought of performing patterning by making the pattern which consists of a compound forming on the 1st layer, and performing alternative etching with this stamp version, no matter it may carry out in what mode, there is no ****.

[0016] Therefore, this invention is not limited to use in the manufacture process of a thin film transistor, either. However, it is more desirable to use for manufacture of semiconductor devices with which dimensional accuracy is not demanded comparatively, such as a thin film transistor, a solar battery, and various sensors, rather than it uses an MOS transistor etc. for manufacture of the semiconductor device which requires dimensional accuracy, since the patterning approach concerning this invention has the property in which it is difficult to raise dimensional accuracy compared with the photolithography method in order to contact the substrate for patterning physically.

[0017]

[Effect of the Invention] After performing the imprint of a pattern in the form of generation of a compound using the substrate for patterning, in order to perform patterning by performing alternative etching according to the patterning approach of the semiconductor device applied to this invention as above, a simpler process can perform patterning.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the phase in early stages of the production process of a general thin film transistor.
[Drawing 2] It is the sectional view showing the condition of having formed three layers, following the condition which shows in drawing 1 .
[Drawing 3] In the condition which shows in drawing 2 , it is the sectional view showing the 1st step which carries out patterning of the etching stopper layer 5 by the approach concerning this invention.
[Drawing 4] It is the sectional view showing a condition when the 1st step shown in drawing 3 is completed.
[Drawing 5] It is the sectional view showing the 2nd step of patterning concerning this invention performed following the 1st step shown in drawing 3 .
[Drawing 6] In the condition which shows in drawing 5 , it is the sectional view showing the 1st step which carries out patterning of the intrinsic-semiconductor layer 4 by the approach concerning this invention.
[Drawing 7] It is the sectional view showing a condition when the 1st step shown in drawing 6 is completed.
[Drawing 8] It is the sectional view showing the 2nd step of patterning concerning this invention performed following the 1st step shown in drawing 6 .
[Drawing 9] In the condition which shows in drawing 8 , it is the sectional view showing the condition of having formed the impurity dope layer 6 further.
[Drawing 10] In the condition which shows in drawing 9 , it is the sectional view showing the 1st step which carries out patterning of the impurity dope layer 6 by the approach concerning this invention.
[Drawing 11] It is the sectional view showing a condition when the 1st step shown in drawing 10 is completed.
[Drawing 12] It is the sectional view showing the 2nd step of patterning concerning this invention performed following the 1st step shown in drawing 10 .
[Drawing 13] In the condition which shows in drawing 12 , it is the sectional view showing the condition of having formed the layer of further some and having constituted a part for the principal part of a thin film transistor.
[Description of Notations]
1 -- Glass substrate
2 -- Gate electrode
3 -- Insulating layer

4 -- Intrinsic-semiconductor layer
4a -- Silicide section
4b -- Channel layer
5 -- Etching stopper layer
5a -- Silicide section
5b -- Etching stopper section
6 -- Impurity dope layer
6a -- Silicide section
6b -- Drain side dope layer
6c -- Source side dope layer
7a -- Drain electrode layer
7b -- Source electrode layer
8 -- Display electrode layer
21, 22, 23 -- Substrate for patterning
31, 32, 33 -- Silicide formation ingredient layer